

## CLAIMS

We claim:

- a) 1            1.    A programmable logic device comprising:
  - a) 2            volatile memory adapted to configure the programmable logic
  - a) 3            device for its intended function based on configuration data
  - a) 4            stored by the volatile memory;
  - a) 5            non-volatile memory adapted to store data which is
  - a) 6            transferable to the volatile memory to configure the
  - a) 7            programmable logic device;
  - a) 8            a first data port adapted to receive external data for
  - a) 9            transfer into either the volatile memory or the non-volatile
  - ) 10           memory; and
  - ) 11           a second data port adapted to receive external data for
  - ) 12           transfer into either the volatile memory or the non-volatile
  - ) 13           memory.
- a) 1           2.    The programmable logic device of Claim 1, further
- a) 2           comprising control logic adapted to transfer the data from the
- a) 3           non-volatile memory to the volatile memory to configure the
- a) 4           programmable logic device.
- a) 1           3.    The programmable logic device of Claim 1, further
- a) 2           comprising core logic adapted to be configured by the
- a) 3           configuration data stored in the volatile memory.

a) 1           4.     The programmable logic device of Claim 1, wherein the  
a) 2 volatile memory comprises static random access memory and the  
a) 3 non-volatile memory comprises flash memory.

a) 1           5.     The programmable logic device of Claim 1, wherein the  
a) 2 non-volatile memory is further adapted to store security bits  
a) 3 that can be set to prevent unauthorized reading of the data from  
a) 4 the programmable logic device.

a) 1           6.     The programmable logic device of Claim 1, wherein the  
a) 2 first data port is a JTAG port and the second data port is a CPU  
a) 3 port.

a) 1           7.     The programmable logic device of Claim 6, wherein the  
a) 2 first data port supports an IEEE 1149.1 standard, with the  
a) 3 external data transferred to the non-volatile memory and/or the  
a) 4 volatile memory via an IEEE 1532 programming mode or to the non-  
a) 5 volatile memory via a background programming mode.

a) 1           8.     The programmable logic device of Claim 6, wherein the  
a) 2 external data is transferred through the second data port to the  
a) 3 volatile memory via a system configuration mode, to the non-  
a) 4 volatile memory directly, and/or to the non-volatile memory via  
a) 5 a background programming mode.

a) 1            9.    The programmable logic device of Claim 1, wherein the  
a) 2 programmable logic device further supports reading back of the  
a) 3 configuration data stored in the volatile memory and/or the data  
a) 4 stored in the non-volatile memory for verification.

a) 1            10.   The programmable logic device of Claim 9, wherein the  
a) 2 programmable logic device further supports the reading back  
a) 3 while the programmable logic device performs its intended  
a) 4 function based on the configuration data stored by the volatile  
a) 5 memory.

a) 1            11.   The programmable logic device of Claim 1, wherein the  
a) 2 programmable logic device supports transfer of the external data  
a) 3 to the non-volatile memory while the programmable logic device  
a) 4 is operable to perform its intended logic functions.

a) 1            12. A programmable device comprising:

a) 2            static random access memory adapted to configure the

a) 3            programmable device for its intended function based on

a) 4            configuration data stored by the static random access memory;

a) 5            flash memory adapted to store data which is transferable to

a) 6            the static random access memory to configure the programmable

a) 7            device;

a) 8            a JTAG port adapted to receive external data for transfer

a) 9            into either the static random access memory or the flash memory;

) 10           a CPU port adapted to receive external data for transfer

) 11           into either the static random access memory or the flash memory;

) 12           and

) 13           means for transferring the external data received by the

) 14           JTAG port or the CPU port to the static random access memory or

) 15           the flash memory.

a) 1           13. The programmable device of Claim 12, wherein the means

a) 2           comprises:

a) 3           a background mode adapted to transfer the external data

a) 4           from the JTAG port to the flash memory or transfer the external

a) 5           data from the CPU port to the flash memory;

a) 6           a programming mode adapted to transfer the external data

a) 7           from the JTAG port to the flash memory and/or to the static

a) 8           random access memory; and

a) 9           a system configuration mode adapted to transfer the

) 10           external data from the CPU port to the static random access

) 11           memory.

a) 1            14.    The programmable device of Claim 13, wherein the  
a) 2 background mode and the programming mode are further adapted to  
a) 3 support readback of data stored in the flash memory and the  
a) 4 static random access memory.

a) 1            15.    The programmable device of Claim 13, wherein the JTAG  
a) 2 port supports an IEEE 1149.1 standard and the programming mode  
a) 3 supports an IEEE 1532 standard.

a) 1            16.    The programmable device of Claim 12, further  
a) 2 comprising control logic adapted to transfer the data from the  
a) 3 flash memory to the static random access memory to configure the  
a) 4 programmable device.

a) 1            17.    The programmable device of Claim 12, further  
a) 2 comprising core logic adapted to be configured by the data  
a) 3 stored in the static random access memory.

a) 1            18.    A method of providing programming options for a  
a) 2            programmable device, the method comprising:  
  
a) 3            providing a background mode for transferring external data  
a) 4            via a first data port or a second data port to non-volatile  
a) 5            memory;  
  
a) 6            providing a direct mode for transferring the external data  
a) 7            via the second data port to the non-volatile memory; and  
  
a) 8            providing a system configuration mode for transferring the  
a) 9            external data via the second data port to volatile memory,  
) 10           wherein the volatile memory is adapted to configure the  
) 11           programmable device.

a) 1            19.    The method of Claim 18, wherein the background mode is  
a) 2            further adapted to readback the external data stored in the non-  
a) 3            volatile memory and the volatile memory.

a) 1            20.    The method of Claim 18, wherein the first data port is  
a) 2            adapted to support a JTAG standard and the second data port is  
a) 3            adapted to provide a CPU interface.

a) 1            21.    The method of Claim 18, further comprising providing a  
a) 2            programming mode for transferring the external data via the  
a) 3            first data port to the non-volatile memory or to the volatile  
a) 4            memory.

a) 1            22.    The method of Claim 21, wherein the programming mode  
a) 2            is further adapted to readback the external data stored in the  
a) 3            non-volatile memory and the volatile memory

a) 1            23.    The method of Claim 21, wherein the programming mode  
a) 2            is further adapted to support an IEEE 1532 standard.

a) 1            24.    The method of Claim 18, further comprising providing a  
a) 2            transfer mode for transferring the external data stored in the  
a) 3            non-volatile memory to the volatile memory.

a) 1            25.    A programmable logic device comprising:

a) 2            volatile memory adapted to configure the programmable logic  
a) 3            device for its intended function based on configuration data  
a) 4            stored by the volatile memory;

a) 5            non-volatile memory adapted to store data which is  
a) 6            transferable to the volatile memory to configure the  
a) 7            programmable logic device; and

a) 8            a CPU port adapted to receive external data for transfer  
a) 9            into either the volatile memory or the non-volatile memory.

a) 1            26.    The programmable logic device of Claim 25, wherein the  
a) 2            volatile memory comprises static random access memory and the  
a) 3            non-volatile memory comprises flash memory.

a) 1            27.    The programmable logic device of Claim 25, wherein the  
a) 2 programmable logic device supports transfer of the external data  
a) 3 through the CPU port to the non-volatile memory while the  
a) 4 programmable logic device is operable to perform its intended  
a) 5 logic functions.

a) 1            28.    The programmable logic device of Claim 25, further  
a) 2 comprising a JTAG port adapted to receive external data for  
a) 3 transfer into either the volatile memory or the non-volatile  
a) 4 memory.

a) 1            29.    The programmable logic device of Claim 28, wherein the  
a) 2 data stored in the volatile memory is transferable directly to  
a) 3 the non-volatile memory.

a) 1            30.    The programmable logic device of Claim 28, wherein the  
a) 2 data stored in either the volatile memory or the non-volatile  
a) 3 memory is transferable out of the programmable logic device via  
a) 4 the CPU port or the JTAG port and transferable into the non-  
a) 5 volatile memory or the volatile memory via the JTAG port or the  
a) 6 CPU port, respectively, to complete a cross port transfer of the  
a) 7 data.



a) 1            31.    A method of providing data transfer options for a  
a) 2    programmable logic device, the method comprising:  
  
a) 3            providing a CPU port adapted to receive external data for  
a) 4    transfer into either volatile memory or non-volatile memory of  
a) 5    the programmable logic device, wherein data stored in the  
a) 6    volatile memory configures the programmable logic device; and  
  
a) 7            providing data registers adapted to transfer data stored in  
a) 8    the non-volatile memory to the volatile memory and to transfer  
a) 9    data stored in the volatile memory to the non-volatile memory.

a) 1            32.    The method of Claim 31, wherein the volatile memory  
a) 2    comprises static random access memory and the non-volatile  
a) 3    memory comprises flash memory.

a) 1            33.    The method of Claim 31, further comprising providing a  
a) 2    JTAG port adapted to receive the external data for transfer into  
a) 3    either the volatile memory or the non-volatile memory of the  
a) 4    programmable logic device.

a) 1            34.    The method of Claim 33, wherein the CPU port and the  
a) 2    JTAG port provide cross port data transfer capability between  
a) 3    the volatile memory and the non-volatile memory.

a) 1            35.    The method of Claim 31, wherein the programmable logic  
a) 2    device supports transfer of the external data through the CPU  
a) 3    port to the non-volatile memory while the programmable logic  
a) 4    device is operable to perform its intended logic functions.